

# Bang-Bang Charge Control for LLC Resonant Converters

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**Abstract**—This paper proposes a Bang-Bang Charge Control (BBCC) method for LLC resonant converters. It utilizes the series resonant capacitor to directly control the cycle-by-cycle input electric quantity, thus can provide very fast dynamic performance in all input and output conditions. The proposed method can be extended to other topologies that include a series capacitor.

## I. INTRODUCTION

The LLC resonant topology [1-4] emerged in recent years. It has been adopted in flat-panel TVs, laptop adapters, computers, and many applications due to its high efficiency advantages. However, the small-signal transfer function of voltage-mode LLC converters vary with input voltage and load current. It changes between a 1<sup>st</sup> order system and a 2<sup>nd</sup> order system in different operating conditions [5]. The 2<sup>nd</sup> order scenario puts constraints to the compensator design, and thus limits the loop bandwidth [6].

Average current-mode control for LLC converters [7, 8] provides constant dynamic performance at different input voltages. However, it only removes the impact of input voltage variation, but does not show significant bandwidth improvement compared to voltage-mode LLC converters. The major limitation is imposed by the current sensing circuitry because: (a) the average current signal must be derived through rectification and low-pass filtering, thus the current loop is several times slower than the switching frequency; (b) the voltage loop must be several times slower than the current loop; (c) the sensed resonant current also include the circulation current, thus does not truthfully reflect the output current level.

Simplified optimal trajectory control [9] introduces a nonlinear controller which only takes effect when a load transient occurs. The nonlinear controller helps the LLC resonant tank take a short path to the steady state. However, the algorithm is derived under the assumption that the switching frequency equals the resonant frequency, which is not always true. Especially, when input voltage is not at the nominal value, the switching frequency must deviate

considerably from the resonant frequency. Also, the algorithm is too complex for on-line computing.

Charge control is proposed as early as in [10-12]. It utilizes a current transformer and a resettable integrator to sense the input charge of each switching cycle, which is costly and not suitable for integration. The same concept is employed in [13] for LLC converters, but its charge sensing scheme relies on a series resistor, which is lossy and unreliable.

This paper proposes a new Bang-Bang Charge Control (BBCC) method for resonant converters. It utilizes the series resonant capacitor as an integrator of the input current, thus cycle-by-cycle input charge is directly controlled without current sensing. As a result, very fast dynamic performance is achieved in all operating conditions with a simple first order compensator.

Half-bridge LLC resonant converter is used as an example in this paper; but the proposed method can be extended to other topologies that include a series capacitor. This paper is organized as follows: Section II explains the operation theory and the control mechanism; Section III discusses the small-signal characteristics; Section IV demonstrates the experimental results; and Section V concludes the paper.

## II. OPERATION THEORY AND CONTROL MECHANISM

The proposed BBCC method is based on the physics that the input electric quantity of each switching cycle can be derived from the series resonant capacitor voltage. The theory is illustrated below, and the control mechanism of the proposed BBCC method follows.

### A. Operation Theory

The input current from a voltage source to a resonant power stage often consists of forward current and reverse current due to the reactive resonant tank. The voltage across the series resonant capacitor is an integral of the resonant tank current, thus the capacitor voltage's variation during an energy exchange period reflects the net input electric

quantity of a switching cycle. Referring to Fig. 1, the energy exchange period for half-bridge resonant topologies begins when the low-side switch is turned off, at which instant the resonant current begins to flow back to the input voltage source; the energy exchange period ends when the high-side switch is turned off, shortly after which the high-side junction capacitance is charged to the input voltage and the input current stops. Fig. 2 shows typical waveforms of half-bridge LLC converters. The energy exchange period can be identified from the input current waveform  $i_{Q1}$ : negative input electric quantity occurs from the low-side switch turn-off point  $t_{Loff}$  to the zero-crossing point  $t_c$ ; and positive input electric quantity occurs from  $t_c$  to the high-side switch turn-off point  $t_{Hoff}$ . The net input electric quantity can be calculated from the  $C_s$  voltage,  $v_{Cs}$ , at  $t_{Loff}$  instant and  $t_{Hoff}$  instant, as derived in (1).

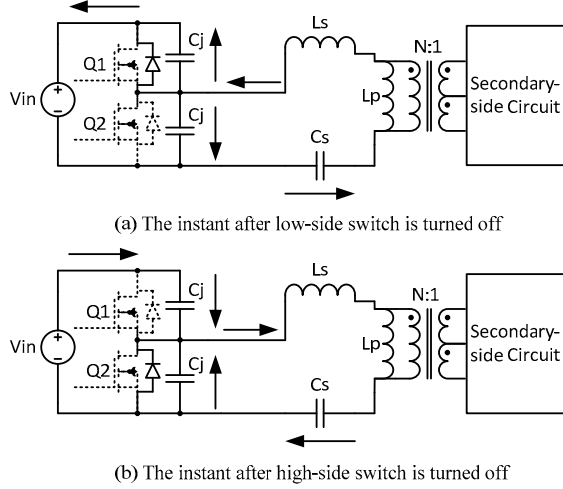


Fig. 1. Initial and end instants of an energy exchange period.

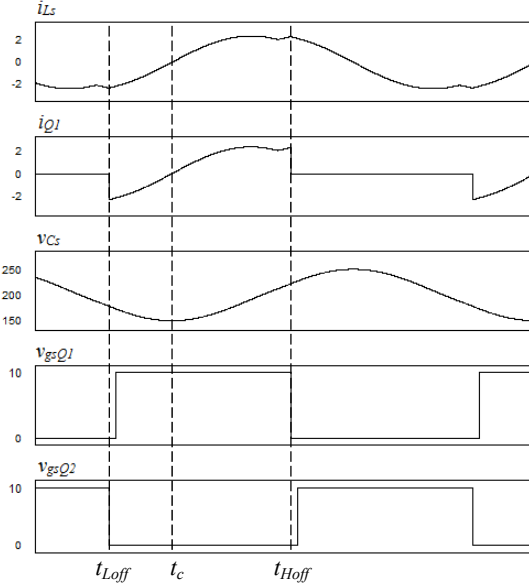


Fig. 2. Typical waveforms of half-bridge LLC converter.

$$\begin{aligned}
 Q_{net} &= Q_{neg} + Q_{pos} \\
 &= C_s [v_{Cs}(t_c) - v_{Cs}(t_{Loff})] + C_s [v_{Cs}(t_{Hoff}) - v_{Cs}(t_c)] \quad (1) \\
 &= C_s [V_{Cs}(t_{Hoff}) - V_{Cs}(t_{Loff})]
 \end{aligned}$$

A closer inspection reveals that the electric quantity resulted from the MOSFETs' junction capacitances,  $C_j$ , should be taken into account. Referring to Fig. 1, shortly after  $t_{Loff}$ , the low-side junction capacitance is charged from 0V to  $V_{in}$  by the resonant current. In (1), this portion of electric quantity is considered as negative electric quantity back to the voltage source; in fact, it stays in the power stage; therefore it should be deducted from the negative input electric quantity. Similarly, after  $t_{Hoff}$ , the input current continues to flow until the high-side junction capacitance is charged from 0V to  $V_{in}$ . This portion of electric quantity is not considered in (1); therefore, it should be added to the positive input electric quantity. As a result, the exact net input charge of a switching cycle is derived in (2), and the consequent input power is derived in (3). Assuming the efficiency loss is negligible, the input power equals to the output power.

$$Q_{net} = C_s [v_{Cs}(t_{Hoff}) - v_{Cs}(t_{Loff})] + 2C_j V_{in} \quad (2)$$

$$P_{in} = V_{in} C_s f_s [v_{Cs}(t_{Hoff}) - v_{Cs}(t_{Loff})] + 2C_j f_s V_{in}^2 \quad (3)$$

Equation (2) and (3) reveals that the input charge of each switching cycle can be derived from the series capacitor voltage at the turn-off points, namely,  $v_{Cs}(t_{Hoff})$  and  $v_{Cs}(t_{Loff})$ , which in turn determine the input power. For half-bridge topologies, the  $C_s$  voltage waveform is symmetrical to one half of the input voltage; therefore  $v_{Cs}(t_{Hoff})$  and  $v_{Cs}(t_{Loff})$  have a relation described in (4).

$$\begin{aligned}
 \frac{V_{in}}{2} - v_{Cs}(t_{Loff}) &= v_{Cs}(t_{Hoff}) - \frac{V_{in}}{2} \quad (4) \\
 \Rightarrow v_{Cs}(t_{Hoff}) + v_{Cs}(t_{Loff}) &= V_{in}
 \end{aligned}$$

## B. Control Mechanism

The proposed BBCC directly control  $v_{Cs}(t_{Hoff})$  and  $v_{Cs}(t_{Loff})$  as thresholds to trigger MOSFETs switching, instead of using a voltage-controlled oscillator as in conventional resonant converters. As a result, the input charge of each switching cycle is directly controlled without current sensing. The core structure of a BBCC controller is illustrated in Fig. 3. The operation waveforms are shown in Fig. 4. The description is as follows.

The input voltage and the series capacitor voltage are scaled down by the same gain factor,  $K_{sen}$ , and are connected

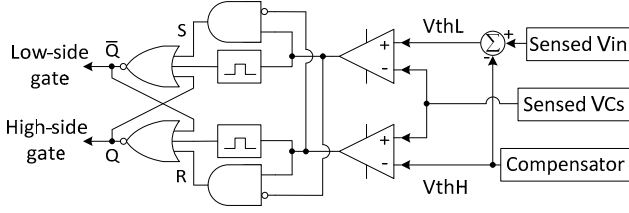


Fig. 3. Core structure of Bang-Bang Charge Controller.

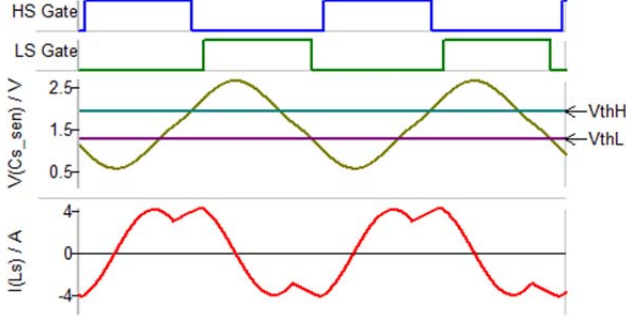


Fig. 4. Operation waveforms of a BBCC controlled LLC converter.

to the BBCC control circuit, shown on the far-right in Fig. 3. The high-side turn-off threshold,  $V_{thH}$ , is generated by the feedback loop compensator. The low-side turn-off threshold,  $V_{thL}$ , is generated by subtracting  $V_{thH}$  from the sensed  $V_{in}$  according to (4).  $V_{thH}$  and  $V_{thL}$  have the following relation with  $v_{Cs}(t_{Hoff})$  and  $v_{Cs}(t_{Loff})$ , respectively:

$$v_{Cs}(t_{Hoff}) = K_{sen} V_{thH} \quad (5)$$

$$v_{Cs}(t_{Loff}) = K_{sen} V_{thL} \quad (6)$$

$V_{thH}$  and  $V_{thL}$  are compared to the sensed  $v_{Cs}$  using two comparators. When the sensed  $v_{Cs}$  is below  $V_{thL}$ , the upper comparator outputs logic HIGH, thus SETs the SR latch shown on the far-left. As a result, the low-side gate is turned off and the high-side gate is turned on. Likewise, when the sensed  $v_{Cs}$  is above  $V_{thH}$ , the lower comparator outputs logic HIGH, thus RESETs the SR latch; then the high-side gate is turned off and the low-side gate is turned on. When the sensed  $v_{Cs}$  is between  $V_{thL}$  and  $V_{thH}$ , both comparators output logic LOW, and the SR latch maintains the previous state.

Light-load operation deserves special considerations. Note that the MOSFETs' junction capacitance also has contribution to the input charge, which is represented by the second term on the right-hand side of (2). Therefore in light load, when the desired input power is lower than that contributed by the junction capacitance,  $V_{thH}$  must be lower than  $V_{thL}$  – effectively reversing the extra energy introduced by the junction capacitance back to the source. In this scenario, the sensed  $v_{Cs}$  can be above  $V_{thH}$  and below  $V_{thL}$  at the same time; then both comparators will output logic HIGH, causing illegal input combination of the SR latch. In

order to solve this problem, monostable blocks are placed between the SR latch and the comparators, converting the comparators' positive steps into positive pulses.

In addition, when the two thresholds are very close to each other, the sensed  $v_{Cs}$  may cross both thresholds within a very short interval. In which case, race condition may occur, and the SR latch's output state after the race condition may be wrong, causing the bang-bang operation to fail. For example, if the sensed  $v_{Cs}$  is already above both thresholds, and the high-side MOSFET is mistakenly turned on, then the sensed  $v_{Cs}$  will never fall below  $V_{thL}$  to trigger the next switching action, and the bang-bang operation will stop. In order to ensure robust operation, the two AND gates, along with their inverting inputs, are used to reinforce the input state of the SR latch: when the sensed  $v_{Cs}$  is above both thresholds, the SR latch receives a steady RESET signal to force turn on the low-side MOSFET; and when the sensed  $v_{Cs}$  is below both thresholds, the SR latch receives a steady SET signal to force turn on the high-side MOSFET. This mechanism also helps determine which MOSFET to be turned on first when the resonant converter resumes from burst mode; the reason is the same as described above.

With above arrangements, the bang-bang operation is robust and reliable.

### III. SMALL-SIGNAL CHARACTERISTICS

The BBCC-controlled resonant converter draws a constant amount of electric quantity from the input voltage source in each switching cycle. The input power is derived in (3). Assuming very high efficiency, the input power equals to the output power. Then the secondary-side current delivered to the load network equals to the input power divided by the output voltage. And the output voltage equals to the secondary-side current multiplied by the load impedance. Using above relations, and substituting (4) and (5) into (3), the output voltage as a function of  $V_{thH}$  can be expressed in (7).

$$V_o(s) = \frac{V_{in} C_s f_s (2K_{sen} V_{thH}(s) - V_{in}) + 2C_j f_s V_{in}^2}{V_o(s)} \cdot \frac{R_L}{1 + sC_o R_L} \quad (7)$$

where  $C_o$  is the output filter capacitor, and  $R_L$  is the load resistance.

Then the small-signal transfer function from  $V_{thH}$  to  $V_o$  can be derived from (7), written in (8).

$$\frac{\hat{v}_o}{\hat{v}_{thH}} = \frac{V_{in} C_s f_s K_{sen}}{V_o} \cdot \frac{R_L}{1 + sC_o R_L} \quad (8)$$

Equation (8) shows that the resonant power stage under BBCC control is a 1<sup>st</sup> order system regardless the input voltage and the load condition. A single pole is determined by the output capacitor and the load resistance, therefore it

will move with respect to the load condition. The input voltage only affects the gain constant.

Strictly speaking, the switching frequency,  $f_s$ , is variable and changes with input voltage and load. However, in the small-signal scale, the frequency variation is very small, and its contribution to the overall dynamic performance is insignificant. Therefore, it can be treated as a constant in (8). Also, because the lowest switching frequency is at least one half of the resonant frequency, its effect on DC gain will be no more than 3dB.

In addition, the assumption that the input power equals to the output power is not valid near the switching frequency. This is because the resonant components store certain amount of energy, and the stored energy changes with different operating conditions. Nevertheless, this effect only appears near the switching frequency, thus it is outside the frequency-of-interest.

Simulation approach is used to verify the above small-signal analysis. The parameters used in simulation are summarized in Table I.

Table I. Simulation parameters.

<b>Topology</b>	Half-bridge LLC resonant
<b>Input voltage (<math>V_{in}</math>)</b>	400V – 300V
<b>Output voltage (<math>V_o</math>)</b>	12V
<b>Transformer turns ratio</b>	20:1
<b>Parallel inductance (<math>L_p</math>)</b>	86 $\mu$ H
<b>Series inductance (<math>L_s</math>)</b>	12 $\mu$ H
<b>Series capacitance (<math>C_s</math>)</b>	36 nF
<b>Junction capacitance (<math>C_j</math>)</b>	1 nF
<b>Output capacitance (<math>C_o</math>)</b>	4 mF
<b>Sensing gain (<math>K_{sen}</math>)</b>	125
<b>Switching frequency (<math>f_s</math>)</b>	125kHz – 170 kHz

Bode plots are drawn for heavy load ( $R_L=0.48\Omega$ ) and light load ( $R_L=2\Omega$ ) at 400V and 300V input conditions, shown in Fig. 5.

As predicted, the control-to-output transfer function shows favorable characteristics for high-performance loop design: (a) the transfer function below the switching frequency is a 1<sup>st</sup> order system in all conditions; (b) the low-frequency pole only moves with load resistance, not with

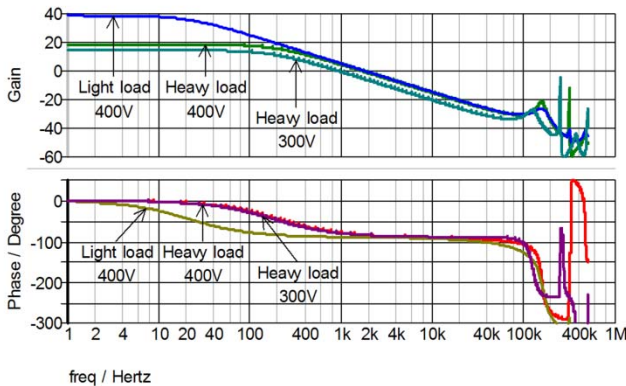


Fig. 5. Bode plots of control-to-output small-signal responses.

the input voltage; (c) a double-pole stays at the switching frequency; it does not move with the load condition as in voltage-mode LLC converters; (d) the gain and phase curves in all operating conditions are remarkably close to each other from kilo-hertz frequency range to the adjacency of switching frequency; this provides an excellent opportunity to achieve optimal loop response in all input and output conditions. The ESR zero is not observed because the ESR of a ceramic capacitor bank is usually very low.

In order to verify the accuracy of the derived small-signal transfer function in (8), comparisons of calculated and measured DC gains and pole frequencies are summarized in Table II and Table III. Table II and Table III demonstrate that the predicted small-signal characteristics by (8) are close to the simulation results. Albeit the prediction of pole frequency at heavy load has slightly larger error, the worst-case scenario for compensator design occurs in light load (the lowest pole frequency); therefore such an error does not affect the design practice.

Table II. Comparison of calculated and simulated DC gains.

Operating condition	DC gain	
	Calculation	Simulation
400V light load	34 dB	38 dB
400V heavy load	21 dB	19 dB
300V heavy load	17 dB	15 dB

Table III. Comparison of calculated and simulated pole frequencies.

Operating condition	Pole frequency	
	Calculation	Simulation
400V light load	20 Hz	21 Hz
400V heavy load	83 Hz	198 Hz
300V heavy load	83 Hz	174 Hz

Taking advantage of the 1<sup>st</sup> order-system characteristic, a simple Type 2 or a PI controller is sufficient to compensate the BBCC controlled resonant converter. The Bode plots of the above example after Type 2 compensation are shown in Fig. 6. A low-frequency zero is placed at 10 Hz to cancel the low-frequency pole of the output filter. A high-frequency pole is placed at 400 kHz, which is intentionally left outside the frequency-of-interest to mimic the behavior of a PI controller.

Theoretically, the worst-case scenario for compensation is at no load, where the load resistance  $R_L$  is infinite, thus the low-frequency pole is at the origin. However, in practice, implementation of burst mode can prevent the linear compensator from operating at very light load; therefore, the worst-case scenario is at the load level at which burst mode is triggered, thus the low-frequency zero can be placed at a higher frequency, e.g. 10 Hz.

The compensation results in Fig. 6 are summarized in Table IV. It shows that the maximum bandwidth can achieve 29 kHz at 400V input condition, and 18 kHz at 300V input condition. In both cases, the bandwidths are about one sixth of their switching frequencies, respectively.

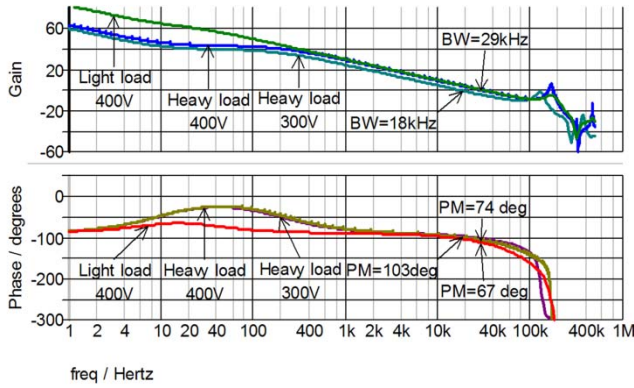


Fig. 6. Bode plots of compensated loop responses.

Table IV. Compensation results shown in Fig. 6.

Operating condition	Bandwidth	Phase margin
400V light load	29 kHz	67°
400V heavy load	29 kHz	74°
300V heavy load	18 kHz	103°

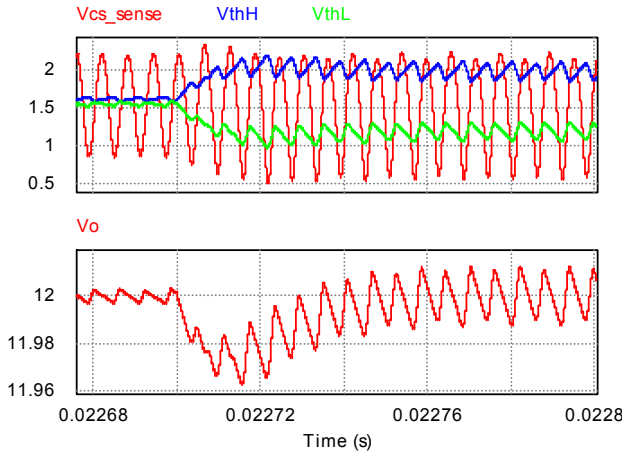


Fig. 7. Load step from 5A to 25A (400V input).

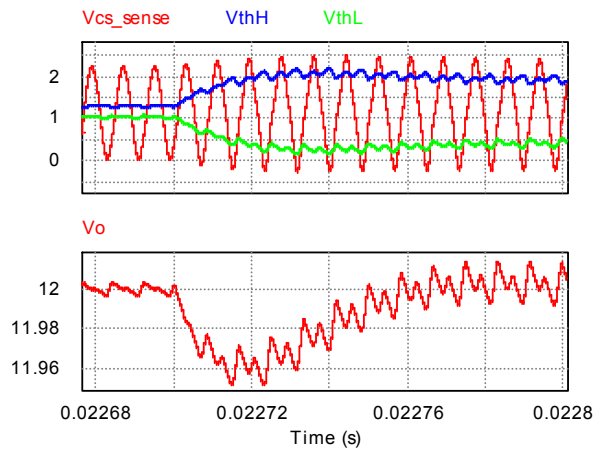


Fig. 8. Load step from 5A to 25A (300V input).

Transient responses simulated at 400V and 300V input voltages are shown in Fig. 7 and Fig. 8. The output voltage is recovered within 7 switching cycles in both cases using the same compensator. It shows that the BBCC control can provide very fast dynamic performance in all operating conditions. The ripples on the threshold signals are due to the output voltage ripple feeding into the compensator. It can be eliminated if use a digital controller or an analog sample-and-hold.

#### IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The experiment is carried out using a half-bridge LLC converter. The power train parameters are listed in Table V. The system diagram is shown in Fig. 9. A Microchip dsPIC33F DSC is used to implement the ADC, PI controller, soft start, and protections. The output of the PI controller is converted to analog signal by a DAC, and is then processed by an analog circuit to generate the  $V_{thH}$  and  $V_{thL}$  thresholds. The comparator outputs are connected to the BBCC logic. The logic is implemented in an Altera MAX II CPLD. It uses only 37 logic elements. In order to exploit the potential of the BBCC control, a high-speed linear optocoupler circuit [14] is used so that the isolator is not a bottle neck of the loop bandwidth.

Table V. Prototype parameters.

Topology	Half-bridge LLC resonant
Input voltage ( $V_{in}$ )	400V – 300V
Output voltage ( $V_o$ )	12V
Transformer turns ratio	20:1
Parallel inductance ( $L_p$ )	86 $\mu$ H
Series inductance ( $L_s$ )	12 $\mu$ H
Series capacitance ( $C_s$ )	36 nF
Output capacitance ( $C_o$ )	1790 $\mu$ F
Sensing gain ( $K_{sen}$ )	100

The steady state waveforms at 5A and 25A load conditions are shown in Fig. 10 and Fig. 11, respectively. A 200 ns propagation delay can be observed from the waveforms, which is mainly contributed by the gate driver. Note in Fig. 10, the threshold  $V_{thH}$  is lower than  $V_{thL}$ . This is predicted in Section II, meaning that the output power is lower than that contributed by the junction capacitance.

Fig. 12 and Fig. 13 show 5A to 25A load step at 400V and 300V input voltage, respectively. In both cases, the output voltage is recovered within 7 switching cycles. This is an outstanding performance provided by a simple PI controller, and the same superior performance is achieved across the input voltage range. This result is also highly consistent with the simulation results in Fig. 7 and Fig. 8.

Fig. 14 and Fig. 15 show 25A to 5A load step at 400V and 300V input voltage, respectively. The switching operation is suspended when the output voltage exceeds a pre-defined threshold, and is resumed when the output voltage falls back to the reference level. Upon resumption, the PI controller is reset, and the fast loop dynamic can quickly reach the steady state, giving fast and smooth transition.

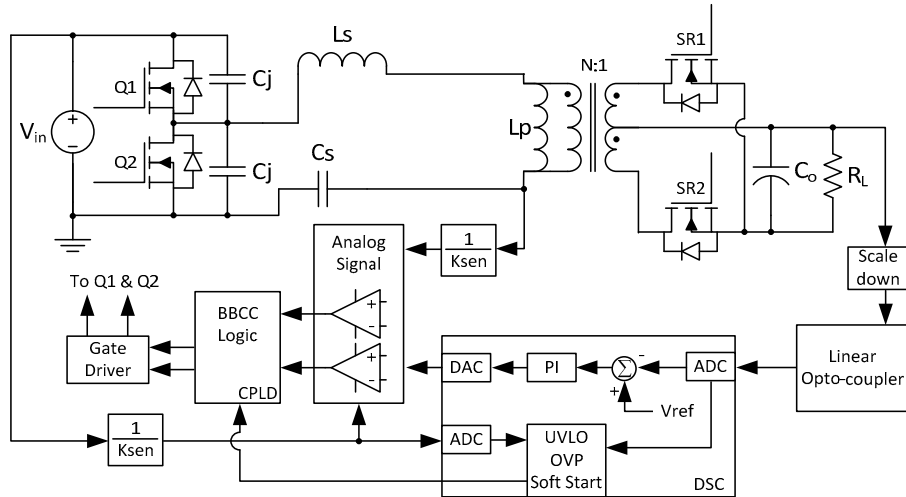


Fig. 9. Block diagram of the BBCC prototype.

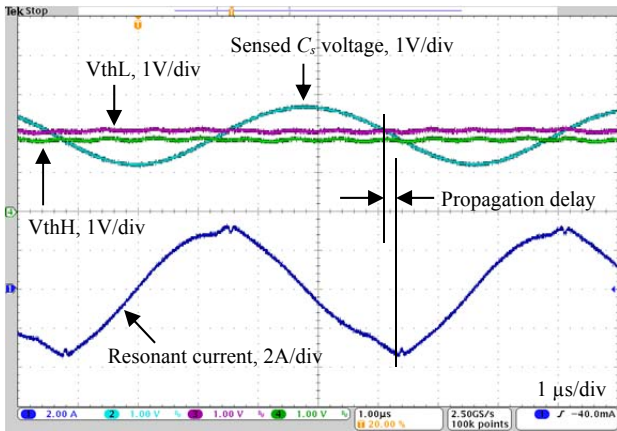


Fig. 10. Steady state at 400V input and 5A load.

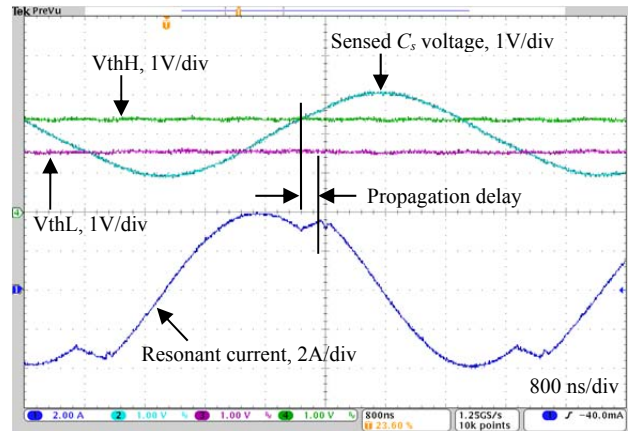


Fig. 11. Steady state at 400V input and 25A load.

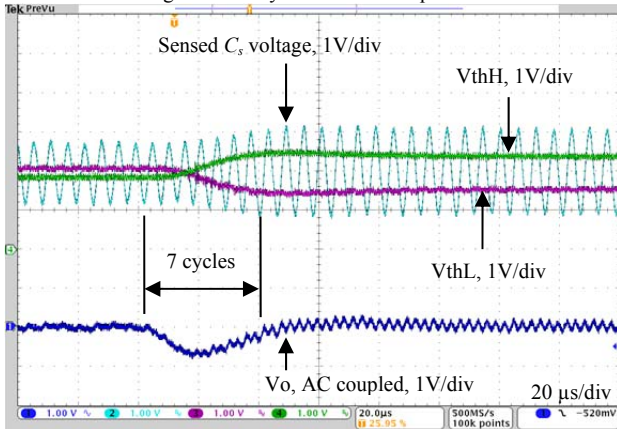


Fig. 12. Load step from 5A to 25A (400V input).

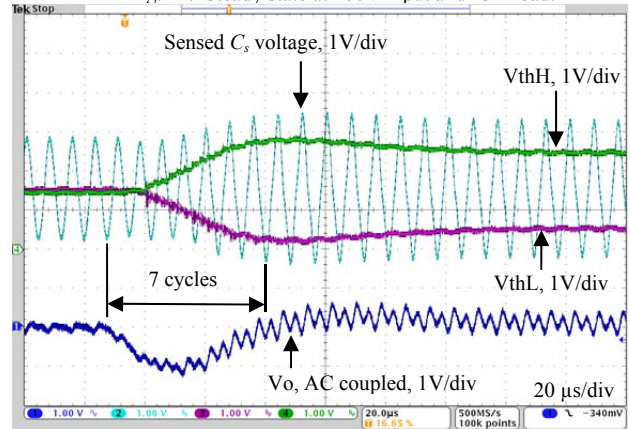


Fig. 13. Load step from 5A to 25A (300V input).

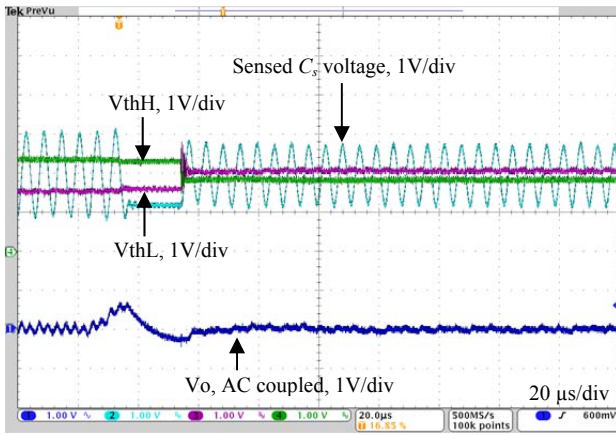


Fig. 14. Load step from 25A to 5A (400V input).

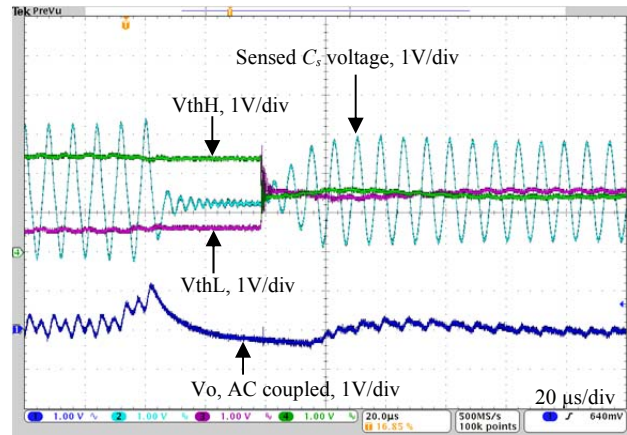


Fig. 15. Load step from 25A to 5A (300V input).

## V. CONCLUSION

A Bang-Bang Charge Control method is proposed for LLC resonant converters. It utilizes the series capacitor voltage to directly control the input charge of each switching cycle, and thus can provide superior dynamic performance in all operating conditions. The control mechanism is simple and low-cost. Small-signal analysis is provided, and is verified by simulation. Experimental results demonstrate the outstanding dynamic performance as predicted by simulation. The proposed method can be extended to other topologies that include a series capacitor.

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